08/522,067, filed August 31, 1995, pending. Application No. 606,212, titled "Apparatus for Performing Multiply-Add Operations on Packed Data," filed Feb 23, 1996, now Pat. No. 6,035,316, which is a CIP of Ser. No. 08/522,067, filed August 31, 1995, pending. Application No. 554,625, titled "An Apparatus for Performing Multiply-Subtract Operations on Packed Data," filed November 6, 1995, now Pat. No. 5,721,892, which is a Continuation of Ser. No. 521,803, filed Aug. 31, 1995, abandoned.

Please replace the paragraph beginning on page 4, line 15 with the following:

Another prior art DSP includes a multiply accumulate instruction that operates on two sets of two values and an accumulation value (See "Digital Signal Processor with Parallel Multipliers", patent number 4,771,379- referred to herein as the "Ando et al." reference). An example of the multiply accumulate instruction for this DSP is shown below in Table 2, where the instruction is performed on the data values A_1, A_2, B_1 and B_2 accessed as Source1-4, repectively.

Please replace the paragraph beginning on page 15, line 10 with the following:

Execution unit 130 is used for executing instructions received by processor 109. In addition to recognizing instructions typically implemented in general purpose processors, execution unit 130 recognizes instructions in packed instruction set 140 for performing operations on packed data formats. Packed instruction set 140 includes instructions for supporting multiply-add and/or multiply-subtract operations. In addition, packed instruction set 140 may also include instructions for supporting a pack operation, an unpack operation, a packed add operation, a packed subtract operation, a packed multiply operation, a packed shift operation, a packed compare operation, a population count operation, and a set of packed logical operations (including packed AND, packed

ANDNOT, packed OR, and packed XOR) as described in "A Set of Instructions for Operating on Packed Data ," filed on Aug. 31, 1995, application number 521,360.

Please replace the paragraph beginning on page 31, line 20 with the following:

In contrast, the disclosed multiply-add and multiply-subtract instructions do not carry forward an accumulation value. As a result, these instructions are easier to use in a wider variety of algorithms. In addition, software pipelining can be used to achieve comparable throughput. To illustrate the versatility of the multiply-add instruction, several example multimedia algorithms are described below. Some of these multimedia algorithms use additional packed data instructions. The operation of these additional packed data instructions are shown in relation to the described algorithms. For a further description of these packed data instructions, see "A Set of Instructions for Operating on Packed Data," filed on Aug. 31, 1995, application number 521,360. Of course, other packed data instructions could be used. In addition, a number of steps requiring the use of general purpose processor instructions to manage data movement, looping, and conditional branching have been omitted in the following examples.

Please replace Table 6a on page 32 with the following:

Multiply-Add Source1, Source2

r_1	i_1	r_1	i_1	Source1
r_2	$-i_2$	i_2	r_2	Source2
		=		
Real Component: $r_1r_2-i_1i_2$		Imaginary Component: $r_1i_2+r_2i_1$		Result 1

Table 6a